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A COMPARATIVE ANLYSIS OF FREQUENCY SYNTHESIZERS

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ABSTRACT

In this paper various techniques for frequency synthesis are described with their advantages and disadvantages, some design example for frequency synthesis for RF application are then reviewed. The review suggest that direct analog frequency synthesizer gives very pure output spectrum but it is bulky and consumes more power. Direct digital frequency synthesizer has fast locking time, less phase noise but it generate frequencies less than reference frequency. Fractional- N Phase locked loop based frequency synthesizers are best suited in modern communication in terms of low power consumption and high frequency resolution.

KEYWORDS: Direct Analog Frequency Synthsizer, Direct Digial Frequency Synthesizer, Frequency Synthsize, R Phase Locked Loop

INTRODUCTION

Phase-locked loops (PLLs) are a well established and very widely used circuit technique in modern electronic systems, which are used primarily in communication systems. In essence, PLLs are circuits in which the phase of a local oscillator is maintained close (or locked) to the phase of an external (reference) signal. The limited bandwidth available to each user in wireless systems mandates the precise definition of the carrier frequency in both the transmitter and receiver. Therefore the frequency synthesizer becomes ubiquitous in modern communication system because of their remarkable versatility. It generates periodic signals with accurately defined frequencies thus serving as an integral part of RF transmitter and receiver. As an important example, a Phase locked loop (PLL) based frequency synthesizer may be used to generate an output signal whose frequency is programmable and a rational multiple of a fixed input frequency [1-5]. The output of such frequency synthesizers may be used as a local oscillator signal in super-heterodyne transceivers. PLL may also be used to perform frequency modulation and demodulation [6-7], as well as to regenerate the carrier from an input signal with suppressed carrier. PLLs are often part of a very large-scale integrated system on a chip extending their versatility to purely digital systems also.

FREQUENCY SYSTHESIZER

The limited bandwidth available to each user in wireless systems mandates the precise definition of the carrier frequency in both the transmitter and receiver. Frequency synthesizers generate periodic signals with accurately defined frequencies thus serving as an integral part of RF transmitter and receiver.

The term frequency synthesizer generally refers to an active electronic device (Figure 1) that accepts some frequency reference (FREF) input signal of a very stable frequency fref and then generates frequency output as commanded by the frequency command word (FCW), whereby the stability, accuracy, and spectral purity of the output

correlate with the performance of the input reference. The desired value of the output frequency is an FCW multiple of the reference frequency according to the equation.

$$f_{out} = FCW.f_{ref}$$

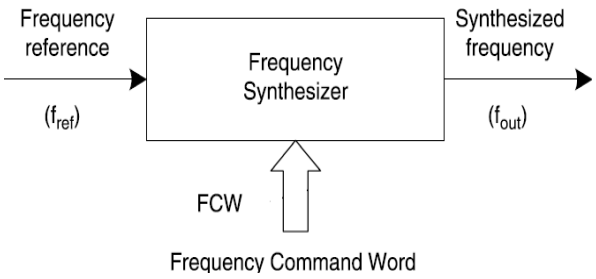

Figure 1: Frequency Synthezer

FREQUENCY SYNTHESIS TECHNIQUES

There are Four major conventional frequency synthesis Techniques:

- Direct analog mix/filter/divide
- Direct digital
- Indirect or phase-locked loop
- **Hybrids:** any combination of the three methods above

Each of these methods has advantages and disadvantages; hence, each application requires selection based on the most acceptable combination of compromises.

Direct Analog Synthesis

Direct analog synthesis, also called mix/filter/divide, uses chain of frequency multipliers, dividers, and other mathematical manipulations to produce the desired new frequency. The desired signal is created directly, without regeneration by mixing base frequencies followed by switching filters as conceptually shown in figure 2. The process is called direct because the error correction process is avoided hence, the quality of the output correlates directly with the quality of the input. The base frequency can be obtained from low-frequency or high-frequency oscillators.

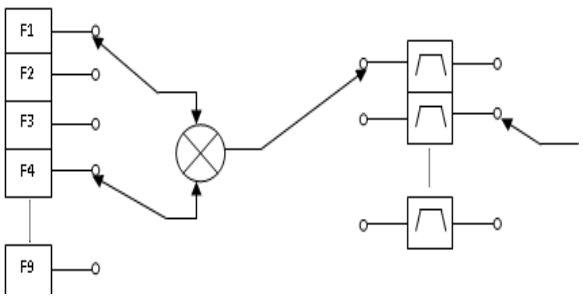

Figure 2: Direct Analog Frequency Synthesis

Direct Digital Synthesis

Direct digital frequency synthesis (DDFS) is the most recently developed frequency synthesis technique, dating from the early 1970s [8]. A DDFS system uses logic and memory to construct the desired output signal digitally, and a data conversion device [a digital-to-analog converter (DAC)] to convert it from the digital to the analog domain [9][10-14]. as shown in Figure 3.

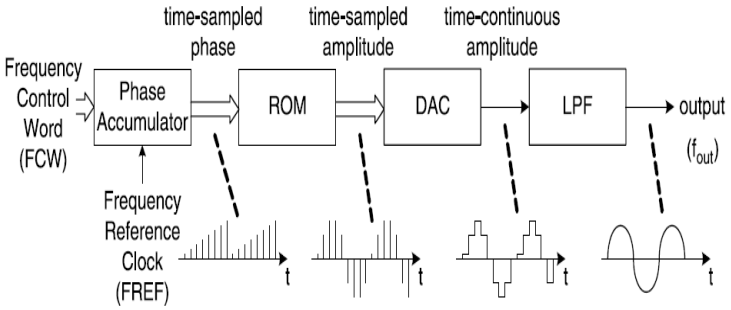

Figure 3: Direct Digital Frequency Syntheses

If the word length of the accumulator be W. For a given frequency command word FCW and clocking (FREF) frequency fref, the output frequency fout of the synthesizer will be

$$f_{out} = \frac{f_{ref}\,(FCW)}{2^w}$$

and the frequency resolution is

$$\Delta f = \frac{f_{ref}}{2^w}$$

Indirect Sysnthesis Using Phase Locking

Phase lock loop(PLL) as a frequency synthesizer is the dominant method in the wireless communication industry[19-21][26]. The ability to execute all PLL functions on a single integrated circuit(IC) has created an economical mass production solution to meet the need of industry. A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals. The overall goal of the PLL is to match the reference and feedback signals in phase—this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. PLL can be categories based on Frequency divider Circuit. Integer-N and Fractional-N frequency synthesizer.

Integer- N Frequency Synthsizer

The frequency division ratio is made variable to set the output Frequency. In the division ratio is integer, Where the VCO frequency is divided using a fixed programmable frequency divider shown in figure 4. In an integer-N frequency synthesizer, the frequency resolution is reference frequency, and its phase-locked loop bandwidth should be set to lower than 1/10 of the reference frequency, and low-frequency VCO phase noise is not effectively suppressed by the PLL loop gain. Therefore, standard frequency synthesizers with integer-N dividers have difficulties in meeting various specifications due to their fundamental tradeoffs between loop bandwidth and channel spacing.

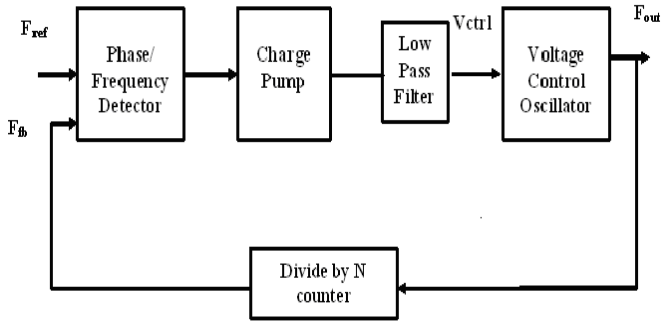

Figure 4: Block Diagram of Integer-N Frequency Synthesizer

Fractional – N Frequency Synthsizer

In Fractional-N frequency synthesizer the division ratio is fractional. Fractional-N frequency synthesizer interpolates fractional division ratios using a multi-modulus divider controlled by a modulator as shown in figure 5. Fractional-N frequency synthesizers can generate any frequencies with wider loop bandwidth using higher reference frequencies than integer-N frequency synthesizers. Therefore, the fractional-N frequency synthesizers offers high switching speed, low phase noise, and finer frequency resolution [27], which are required in most modern wireless systems. Fractional-N frequency-synthesizers techniques are more suitable in the wireless communication system as a local oscillator to generate accurately frequencies [28].

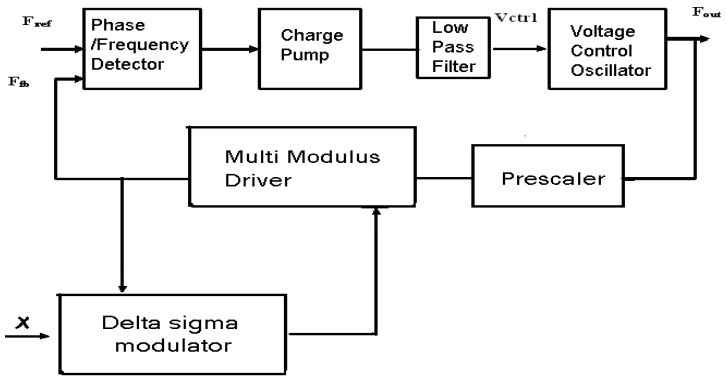

Figure 5: Block Diagram of Fractional-N Frequency Synthesizer

In many recent efforts, fractional frequency division ratios are shown to be interpolated using modulation techniques. For fractional-N frequency synthesis, two types of modulators have been used. One is a single-loop modulator, and the other is a cascaded modulator called MASH. The single-loop modulator has a choice of a single-bit or a multi-bit output depending on the quantity while the MASH architecture outputs only multi-bits. Comparing the output bit patterns of the multi-bit modulator and the MASH, the former can achieve a more desirable noise shaping for frequency synthesis, but the latter offers simpler high-order architecture with no stability problem.

A basic form of a PLL based Fractional -N frequency synthesizer consists of f six main blocks [17]:

- Phase Detector or Phase Frequency Detector (PD or PFD)
- Charge Pump (CP)
- Low Pass Filter (LPF)
- Voltage Controlled Oscillator (VCO)
- Frequency Divider (FD)
- Sigma Delta modulator

Phase Frequency Detector: PFD detector is used to find the phase difference and frequency difference between the input signal and feedback signal from the output of voltage-controlled oscillator. There are three types of PFD such as XOR PFD, D-Flip Flop Phase Frequency Detector, and Gate-Level Phase Frequency Detector

Charge Pump: In the low-pass filter the average value of the PFD output is obtained by depositing charge onto a capacitor during each phase comparison and allowing the charge to decay.

If the output lags the input, speed up the VCO. If the input lags the output, slow down VCO.

Loop Filter: Loop filters translate between the phase detector's measurement signal and the VCO's control voltage(s). The loop filter used with phase frequency detector is simple RC low-pass filter.

Voltage Controlled Oscillator (VCO): VCO is simply the voltage to frequency converter. The frequency of the clock generated is controlled by one or more voltage inputs. There are various type of VCO as Ring Oscillator, LC VCO, Current starved VCO and many more.

Frequency Divider: A frequency divider enables the frequency of the VCO to be some multiple of the reference signal. The divider performs frequency division on the output signal to generate a signal, which has the frequency of the input but the phase of the output.

Sigma Delta Modulator: The multi-modulus frequency divider is controlled by a simple accumulator in traditional fractional-N synthesizer. However, this architecture will cause the fractional spurious problem. These fractional spurious can be reduced and suppressed by a delta-sigma modulator technology [29].The MASH or cascade 1-1-1 modulator is easy to integrate in CMOS and is unconditionally stable. MASH architecture uses a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones. The advantage of this approach is that higher-order noise filtering can be achieved using lower-order modulators. The overall cascaded system should remain stable in contrast to other high-order modulator structures because the MASH lower-order modulators are more stable.

MASH delta-sigma modulator produces a multi-bit output, which used as modulus controller for fractional-N frequency synthesizer. The delta-sigma modulator output controls the instantaneous division modulus of the multi-modulus divider, such that the mean division modulus is N div.

The corresponding phase changes at the divider output are quantized, leading to possible spurious tones and quantization noise. The delta-sigma modulator noise transfer characteristic is known to be high pass in nature and results in very low in-band noise levels, along with higher out-of-band noise levels which can be suppressed by the filtering of the phase-locked loop.

The phase frequency detector, PFD, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates "up" or "down" synchronized signals to the charge pump/ low pass filter.

If the error signal from the PFD is an "up" signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage, Vctrl. On the contrary, if the error signal from the PFD is a "down" signal, the charge pump removes charge from the LPF capacitor, which decreases Vctrl. Vctrl is the input to the VCO.

Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an "up" signal, the VCO speeds up. On the contrary, if a "down" signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thus creating a closed loop frequency control system.

Frequency Synthesis Based on Hybrid Structure

In certain applications it is necessary to combine two (rarely, three) major synthesis techniques such that the best features of each basic method are emphasized [15-17]. Generally, it is a hybrid of DDFS and PLL structures that is used in certain wireless devices.

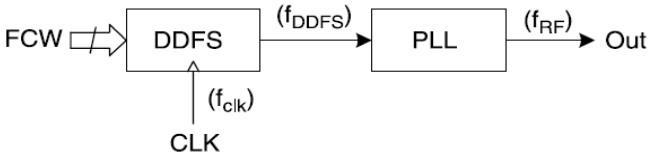

Figure 6: DDFS–PLL Hybrid

As shown in Figure 6, the wideband modulation and fast channel-hopping capability of the DDFS method, which now operates at lower frequency, could be combined with the frequency multiplication property of a PLL that up-converts it to the RF band.

In this section, Advantages and Disadvantages of various frequency synthesizers are tabulated

Table 1: Direct Analog Frequency Synthesizer

Advantage	Disadvantage
Possibility for rapid frequency change	Difficult layout of the circuit
Very pure output spectrum	High power consumption
	Costly
	bulky

Table 2: Direct Digital Frequency Synthesizer

Advantage	Disadvantage
Fast settling time	Fast D/A converters are difficult to make accurately
Continuous – phase frequency switching	Discrete narrow band spurious
Low phase noise	Reference source must operate at a higher frequency than that synthesized
Very high frequency resolution	High power consumption
Very high tuning range	Phase quantization noise problem
Low cost and less complex	Ratio of D/A settling time to cycle time is a limiting factor

Table 3: Indirect Frequency Synthesizer Using PLL

Advantage	Disadvantage
Useful in narrow spacing between operating frequencies	Expensive
Easily configured for complex synthesis using multi loop	High phase noise
Possible to down convert input frequency	Spurious is sever
Possible to generate a jitter free sine wave at the output	Vast amount of filtering required
Phase noise degradation of a signal passing through a filter is possible only if the noise level of the input is very low and if mixers are not optimized	Lock-up time is related to the smallest frequency component

Table 4: Comparison of Various Frctional-N Frequency Synthesizers Based on PLL

	[30]	[31]	[32]	[33]	[34]	[35]
Technology	0.18µm	0.18µm	0.18µm	0.18µm	0.18µm	65nm
Power Supply voltage	1.5V	N/A	2V	1V	1V	N/A
Reference frequency	28MHz	50MHz	20MHz	48 MHz	50MHz	40MHz
Phase noise	-116 dBc/Hz @1MHz	-106.2 dBc/Hz @1MHz	-117.6 dBc/Hz @1MHz	-155 dBc/Hz@ 20MHz	-148 dBc/Hz@ 20MHz	-104 dBc/Hz @40kHz
Power consumption	20mW	61mW	299mW	67mW	110mW	80mW
Die Area	NA	6.25mm^2	4.4mm^2	4.84mm^2	7.29mm^2	0.4mm^2

The designing of fractional-N PLL has been referred by many researchers during the last decade as mentioned in the literature review but few contributions from several researchers are having a considerable impact on this research domain.

Chin – Ying Chen [30] reported fractional-N frequency synthesizer with a MASH delta-sigma modulator. This architecture allows higher reference frequency than the frequency resolution. Phase noise calculated is -116 dBc /Hz at 1MHZ offset frequency which is contributed only by VCO is considered. Frequency resolution step is of the order of 27 kHz is poor.

Pin–En Su and Sudhakar pamarti [31] presented delta- sigma fractional-N synthesizer in which they inserted a phase generator to reduce quantization error they also suggested spur suppression technique. Shih –An yu et al. [32] presented signal source with frequency 125 MHz to 5.2 GHz. chip is fabricated in a 0.18 um SiGe BiCMOS technology. The phase noise performance achieved is – 117.6 dBc/Hz at 1 MHz. die area reported is 4 mm2 which is large. Scott E Menninger and Michael H. Parrott [33] reported a topology with hybrid phase / frequency detector and digital to analog converter for mismatch compensation to perform active cancellation of fractional – N quantization noise.

This design shows high closed loop bandwidth of 1 MHz which is high but consuming nose power of the order of 110mw. Xueyi Yu et al. [34] described a noise filtering method for ΔΣ fractional- N PLL clock generators to reduce out-of-band phase noise and improve short-term jitter performance. A hybrid finite impulse response (FIR) filtering technique based on a semi digital approach enables low-OSR ΔΣ modulation with robust quantization noise reduction despite circuit mismatch and nonlinearity.

A prototype 1-GHz ΔΣ fractional-N PLL is implemented in 0.18 um CMOS. Method effectively suppresses the out-of-band quantization noise, resulting in nearly 30% reduction in short-term jitter. Proposed design showed phase noise -148 dBc/Hz but at the cast of high power consumption and die area. Marzo Zanuso et al. [35] reported a digital sigma data fractional-N frequency synthesizer for 4G communication standards. Design is able to achieve wide loop bandwidth while producing low fractional spurs.

They uses correlation algorithm to correct the phase interpolator mismatches. This architecture relaxes the typical trade off among fractional spurs, noise and loop bandwidth. Reported design resulting in maximum bandwidth 3200 kHz, reference spurs -57 dBc and in band noise -104 dBc/Hz. Sudhakar Pamarti et al. [36] presented fractional N PLL with phase noise cancellation

Technique that and charge pump linearization technique. There Techniques relaxed the fundamental tradeoff between phase noise and band width in conventional fractional – N PLL s reported loop bard with of 460 kHz and phase –noise – 127 dBc/Hz at 3 MHz offset.

CONCLUSIONS

In this paper we have compared and analyzed the recent fractional-N PLLs. It is found that most of frequency synthesizers used fractional-N PLL for various applications. Phase noise, jitter and fractional spur is main concern of designing. It is also found that there is a trade of among phase noise, power dissipation, speed and area. Various designs worked to get best results for all above mentioned parameters

REFERENCES

1. I. Hwang, S. Lee, S. Lee, and S. Kim, “A digitally controlled phase-locked loop with fast locking scheme for clock synthesis application,” ISSCC Dig. Tech. Papers, pp. 168–169, Feb. 2000.
2. D. W. Boerstler, “A low-jitter PLL clock generator for microprocessors with lock range of 340–612 MHz,” IEEE J. Solid State Circuits, vol. 34, pp. 513–519, Apr.1999.

3. V. R. von Kaenel, “A high-speed low-power clock generator for a microprocessor application,” IEEE J. Solid State Circuits, vol. 33, pp. 1634–1639, Nov. 1998.

4. C. Chung and C. Lee, “An all-digital phase-locked loop for high-speed clock generation,” IEEE J. Solid-State Circuits, vol. 38, pp. 347–351, Feb. 2003.

5. P. Nilsson and M. Torkelson, “A monolithic digital clock-generator for on-chip clocking of custom DSP’s,” IEEE J. Solid-State Circuits, vol.31, pp. 700–706, May1996

6. Kobayashi, Kei; Yamada, Hirofumi; Itoh, Hiroshi; Horiuchi, Toshihisa; Matsushige, Kazumi “Analog frequency modulation detector for dynamic force microscopy” IEEE J. Review of Scientific Instruments, Vol. 72 pp. 4383 – 4387. Dec.2001

7. Hao Wei ; Wang Pinglian ; Zhao Hui “The design of an efficient satellite IF PLL PM demodulator with low complexity” 3rd International Conference on Computational Electromagnetics and Its Applications, Proceedings. ICCEA 2004, pp: 316 – 319, 2004

8. J. Tierney, C. Rader, and B. Gold, “A Digital Frequency Synthesizer”, IEEE Trans. Audio Electroacoust, vol. AU-19, Mar. 1971 pp. 48–57.

9. J. Vankka, “Methods of mapping from phase to sine amplitude in direct digital synthesis,” IEEE Trans. Ultrason. Ferroelectr. Freq. Control, vol. 44, no. 2, pp. 526–534, Mar. 1997.

10. Y. Xuefeng, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 12 GHz 1.9 W Direct Digital Synthesizer MMIC Implemented in 0.18um SiGe BiCMOS Technology," Solid-State Circuits, IEEE Journal of, vol. 43, pp. 1384-1393, 2008.

11. S. E. Turner, R. T. Chan, and J. T. Feng, "ROM-Based Direct Digital Synthesizer at 24GHz Clock Freuqency in InP DHBT Technology," IEEE Microwave and Wireless Components Letters, vol. 18, p. 3, 2008.

12. B. Laemmle, C. Wagner, H. Knapp, L. Maurer, and R. Weigel, "A 366mW direct digital synthesizer at 15GHz clock frequency in SiGe Bipolar technology," in Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE, 2009, pp. 415- 418

13. S. E. Turner and D. E. Kotecki, "Direct Digital Synthesizer With Sine-Weighted DAC at 32-GHz Clock Frequency in InP DHBT Technology," Solid-State Circuits, IEEE Journal of, vol. 41, pp. 2284-2290, 2006.

14. G. Xueyang, F. F. Dai, J. D. Irwin, and R. C. Jaeger, "A 5 GHz direct digital synthesizer MMIC with direct modulation and spur randomization," in Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE, 2009, pp. 419-422.

15. H. Ryu; Y. Kim; H. Yu; H. Lee, “ A new triple-controlled type frequency synthesizer using simplified DDFS-driven digital hybrid PLL system” IEEE Tran Consumer Electronics Vol.48, no.1, 2002 , pp. 63–71

16. H. Ryu; Y. Kim; H. Yu; S. Ryu, “Design of DDFS- driven PLL frequency synthesizerwith reduced complexity” IEEE Tran. Consumer Electronics Vol.47, no.1, 2002 , pp. 194 - 198

17. Kun-Sup Kwon; Won-Sang Yoon, “Method to suppress DDFS spurious signals in a frequency-hopping synthesizer with DDFS-driven PLL architecture” IEEE Trans., Ultrasonics, Ferroelectrics and Frequency Control, Vol. 5,no.2, 2010, pp. 299 - 304

18. Hong Chang Yeoh; Jae-Hun Jung; Yun-Hwan Jung; Kwang-Hyun Baek; "A 1.3-GHz 350-mW Hybrid Direct Digital Frequency synthesizer in 90-nm CMOS" IEEE Journal Solid-State Circuits Year: 2010 Vol. 45, No. 9, pp:1845 – 1855

19. Sheen, R. R.- B.; Chen,O.T.-C., " A CMOS PLL - freqency synthsizer for wireless communication systems at 0.9, 1.8, 1.9 and 2.4 GHz" IEEE International Symposium, Circuits and Systems, ISCAS 2001 Vol., 4 2001, pp. 722 – 725

20. Kho, J.; Loh, C.I.; Wui Hung Moo; Chee Seong Fong; Man On Wong, "Extended analysis of SSN effect on phase-locked loop (PLL) circuit" Electrical Design of Advanced Packaging & Systems Symposium, (EDAPS2009),IEEE, 2009,pp.1–4

21. J. Kaiser and T. H. Lin, "A 900 MHz 2.5 mA CMOS frequency synthesizer with an automatic SC tuning loop," IEEE J. Solid-State Circuits,vol. 36, no. 3, pp. 424–430, Mar. 2001.

22. H. C. Luong and C. W. Lo, "A 1.5 V 900 MHz monolithic CMOS fast switching frequency synthesizer for wireless applications," IEEE J. Solid-State Circuits, vol. 37, no. 4, pp. 459–469, Apr. 2002.

23. A. Abidi and E. Hegazi, "17 mW transmitter and frequency synthesizer for 900 MHz GSM fully integrated in 0.35 _m CMOS," IEEE J. Solid-State Circuits, vol. 38, no. 5, pp. 782–792, May 2003.

24. W.Wang and H. C. Luong, "A 0.8-V 4.9-mW 1.2-GHz CMOS fractional-N frequency synthesizer for UHF RFID readers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 9, pp. 2505–2513, Oct. 2008.

25. H.-H. Hsieh, C.-T. Lu, and L.-H. Lu, "A 0.5-V 1.9-GHz low-power phase locked loop in 0.18- μm CMOS," in Porc. Symp. VLSI Circuits, Jun. 2007, pp. 164–165.

26. S. Yu and P. Kinget, "A 0.65 V 2.5 GHz fractional-N frequency synthesizer in 90 nm CMOS," in Proc. ISSCC Dig. Tech. Papers, Feb. 2007,pp. 304–305.

27. B. Miller and B. Conley, "A multiple modulator fractional divider," IEEE the 44th Annual Frequency Control Symposium, pp. 559 -568 May 1990.

28. Mucahit Kozak and E. G. Friedman, "Design and simulation offractional-N PLL frequency synthesizers," ISCAS '04, Vol. 4, pp. 780-783, May 2004.

29. F. M. Gardner, "Charge-pump phase-lock loops," IEEE Trans. Commun., vol. COM-28, no. 11, pp. 1849–1858, Nov. 1980

30. Chin-Ying Chen; Jyh-Jier Ho; Wan-Rone Liou; Hsiao, R.Y.; "A 5.2GHz CMOS fractional-n frequency synthesizer with a MASH delta-sigma modulator" IEEE 51st Midwest Symposium on Circuits and Systems, 2008. MWSCAS 2008.

31. Pin-En Su ; Pamarti, S. ; "A 2-MHz bandwidth Δ-Σ fractional-N synthesizer based on a fractional frequency divider with digital spur suppression" IEEE Radio Frequency Integrated Circuits Symposium (RFIC), pp 413 – 416, 2010.

32. Shih-An Yu ; Baeyens, Y. ; Weiner, J. ; Koc, U.-V. ; Rambaud, M. ; Fang-Ren Liao ;Young-Kai Chen ; Kinget, P.R. ; "A Single-Chip 125-MHz to 32-GHz Signal Source in 0.18- um SiGe BiCMOS" IEEE Journal of Solid-State Circuits, Vol.46, No.3 pp 598 - 614 : March2011

33. S. E. Meninger and M. H. Perrott, "A 1-MHz bandwidth 3.6-GHz 0.18-μm CMOS fractional-N synthesizer utilizing a hybrid PFD/DAC structure for reduced broadband phase noise," IEEE J. Solid-State Circuits, vol. 41, no. 4, pp. 966–980, Apr. 2006.

34. X. Yu, Y. Sun, W. Rhee, and Z. Wang, "An FIR-embedded noise Filtering method for ΔΣ fractional- N PLL clock generators", J. Solid-State Circuits, Vol.44, No.9 pp 2426- 2436, Sep2009.

35. Marzo Zanuso, S. Levantino, Carlo Samori and Andrea L. Lacaita, "A wideband 3.6 GHz digital ΔΣ fractional- N PLL with phase interpolation divider and digital spur cancellation", J. Solid-State Circuits, Vol.46, No.3 pp 627-638, Mar. 2011.